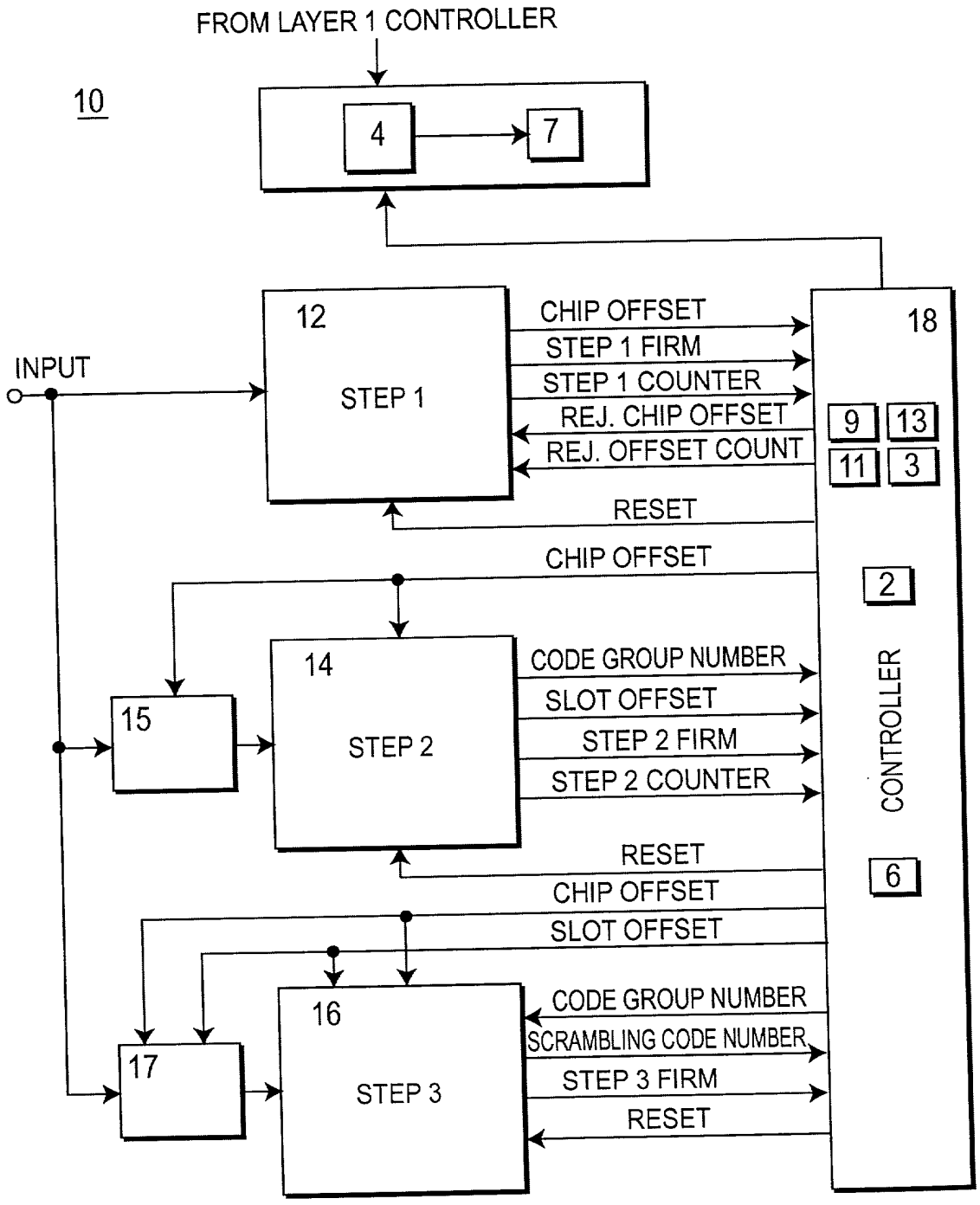
FROM LAYER 1 CONTROLLER
10
4
7
12
STEP 1
INPUT
CHIP OFFSET
STEP 1 FIRM
STEP 1 COUNTER
REJ. CHIP OFFSET
REJ. OFFSET COUNT
RESET
18
9
13
11
3
CHIP OFFSET
2
15
14
STEP 2
CODE GROUP NUMBER
SLOT OFFSET
STEP 2 FIRM
STEP 2 COUNTER
RESET
CONTROLLER
6
CHIP OFFSET
SLOT OFFSET
17
16
STEP 3
CODE GROUP NUMBER
SCRAMBLING CODE NUMBER
STEP 3 FIRM
RESET

FIG. 1

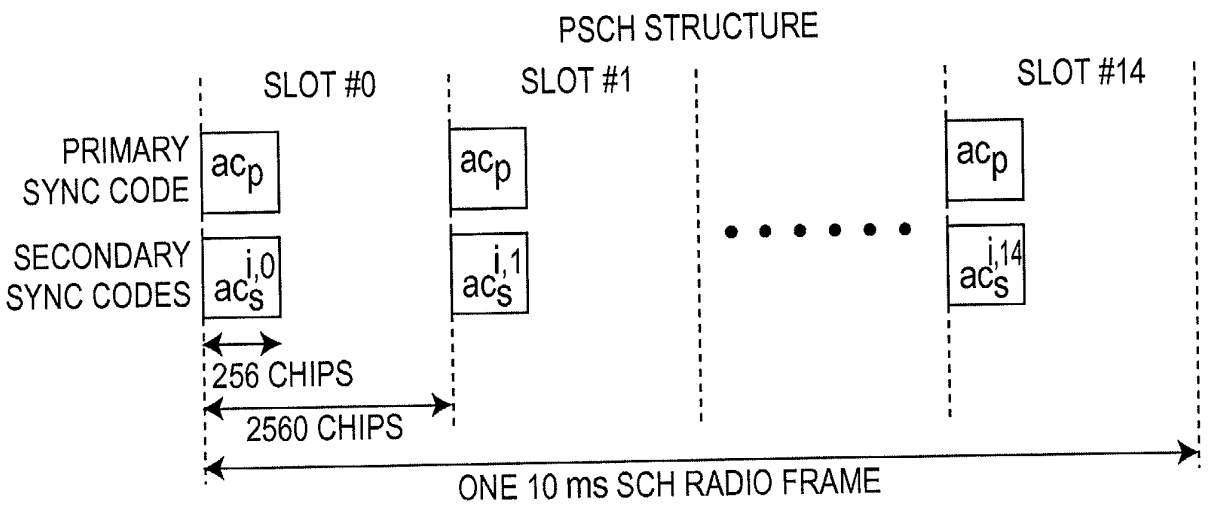
PSCH STRUCTURE
SLOT #0
SLOT #1
SLOT #14
PRIMARY SYNC CODE
SECONDARY SYNC CODES
ac_p
$ac_s^{i,0}$
$ac_s^{i,1}$
$ac_s^{i,14}$
256 CHIPS
2560 CHIPS
ONE 10 ms SCH RADIO FRAME

FIG. 2

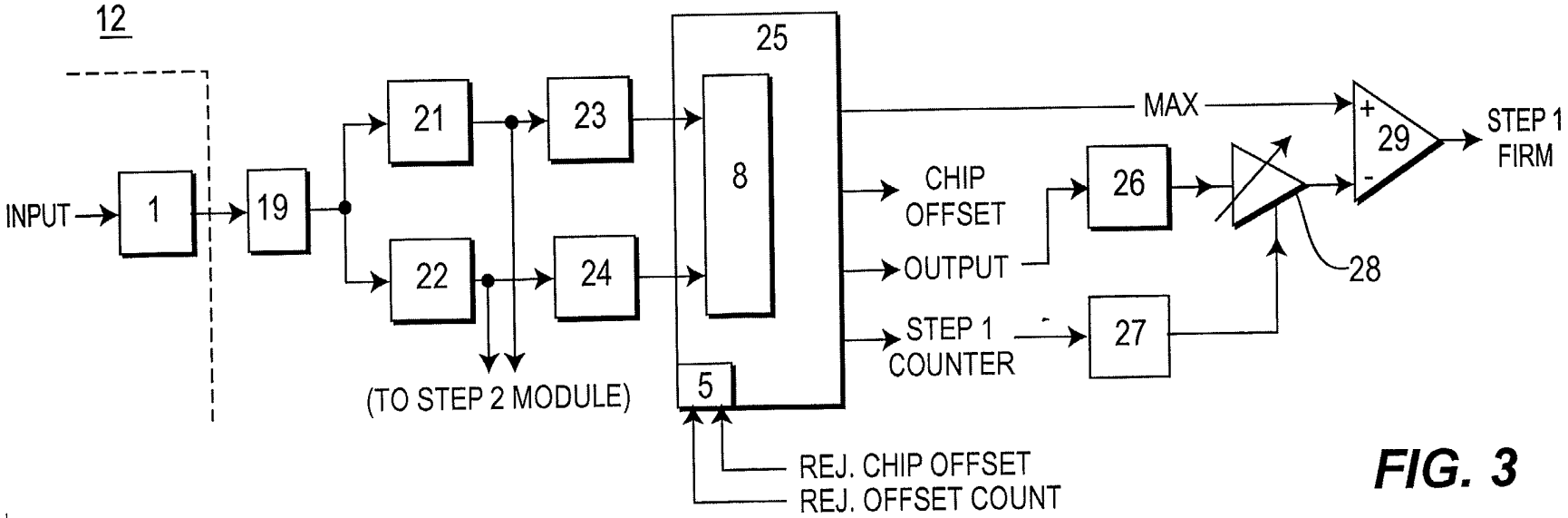
12
INPUT
1
19
21
22
23
24
25
8
5
(TO STEP 2 MODULE)
MAX
CHIP OFFSET
OUTPUT
STEP 1 COUNTER
26
27
28
29
+
-
STEP 1 FIRM
REJ. CHIP OFFSET
REJ. OFFSET COUNT

FIG. 3

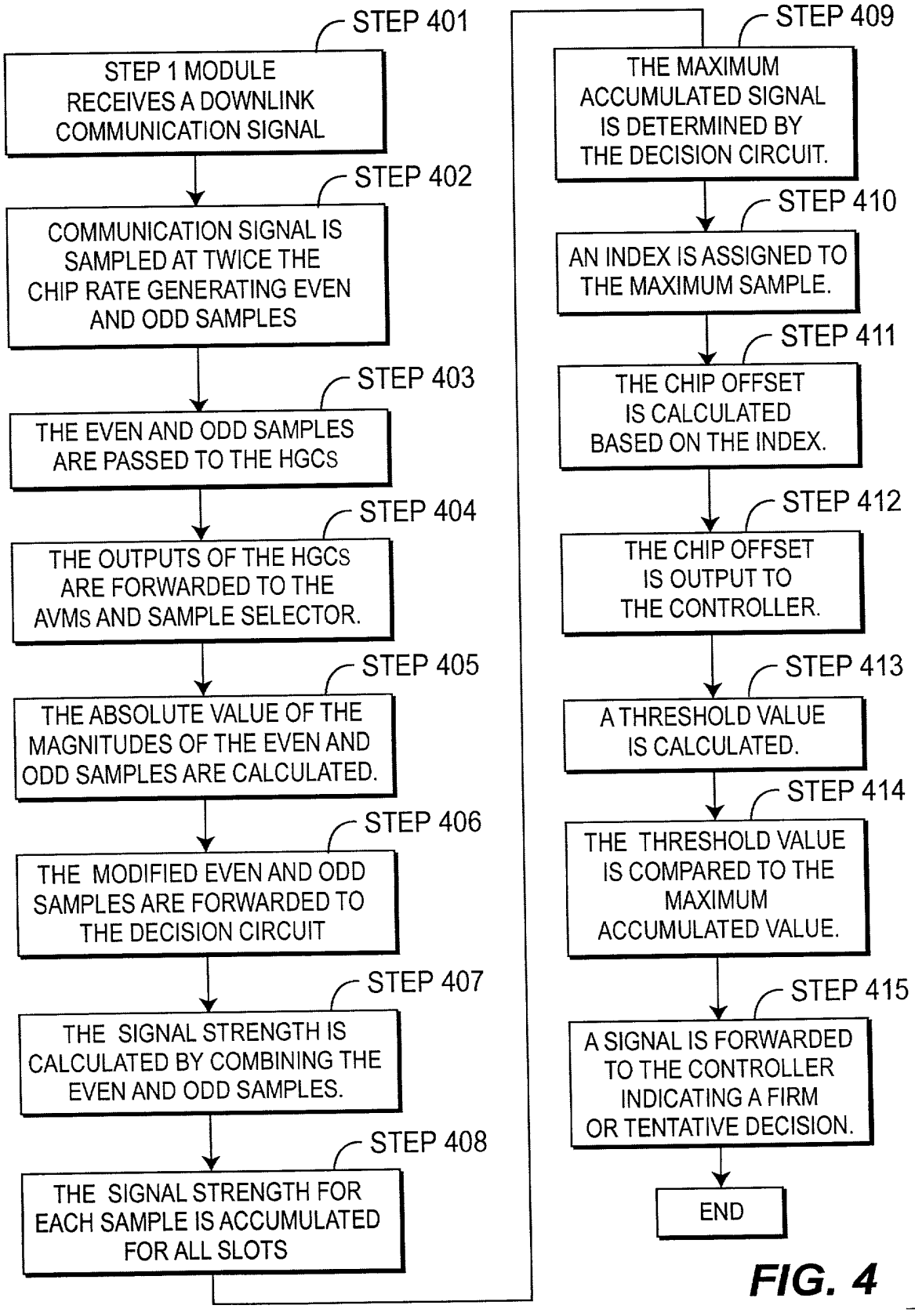

FIG. 4

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20220'96E800T

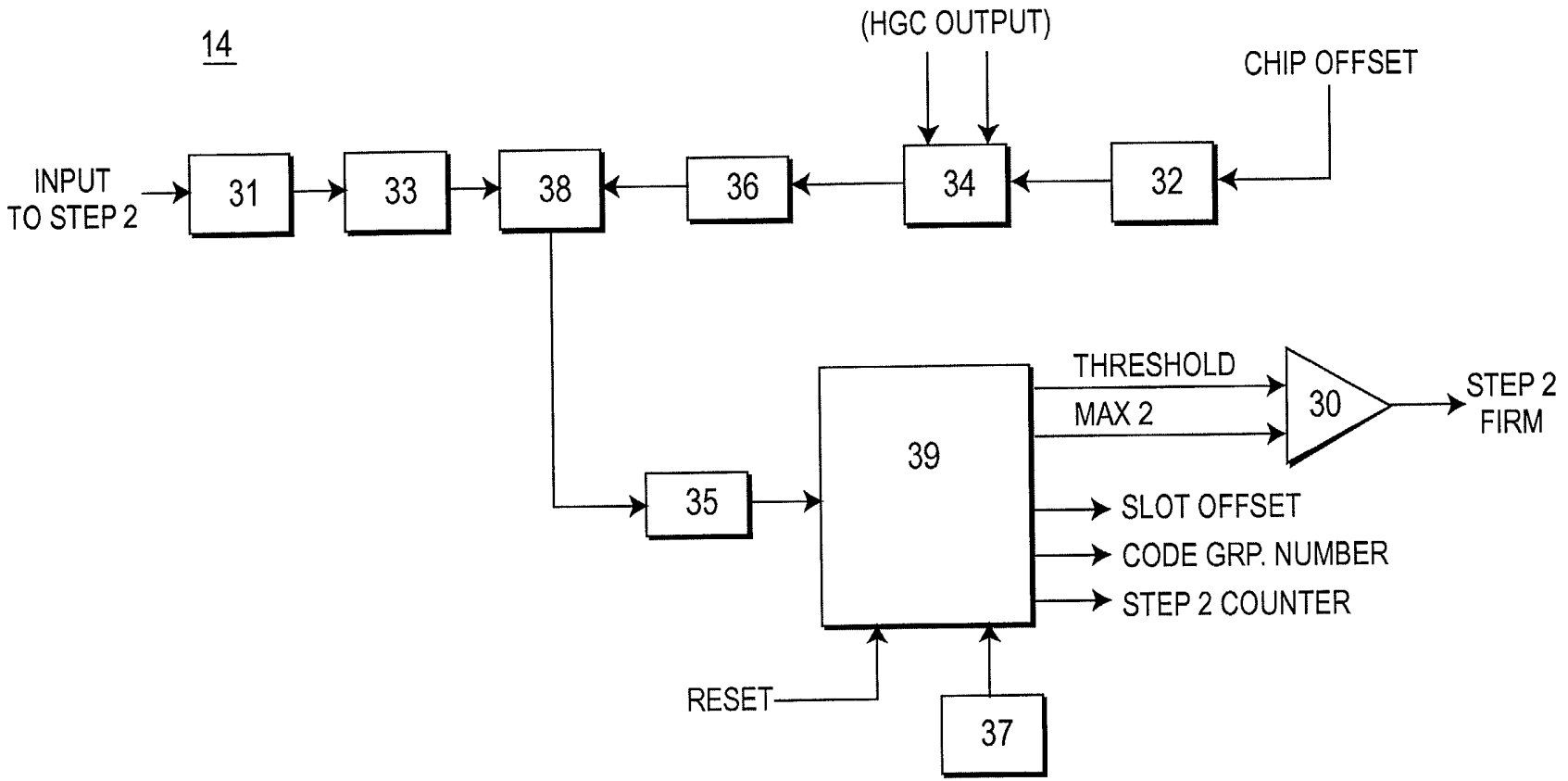
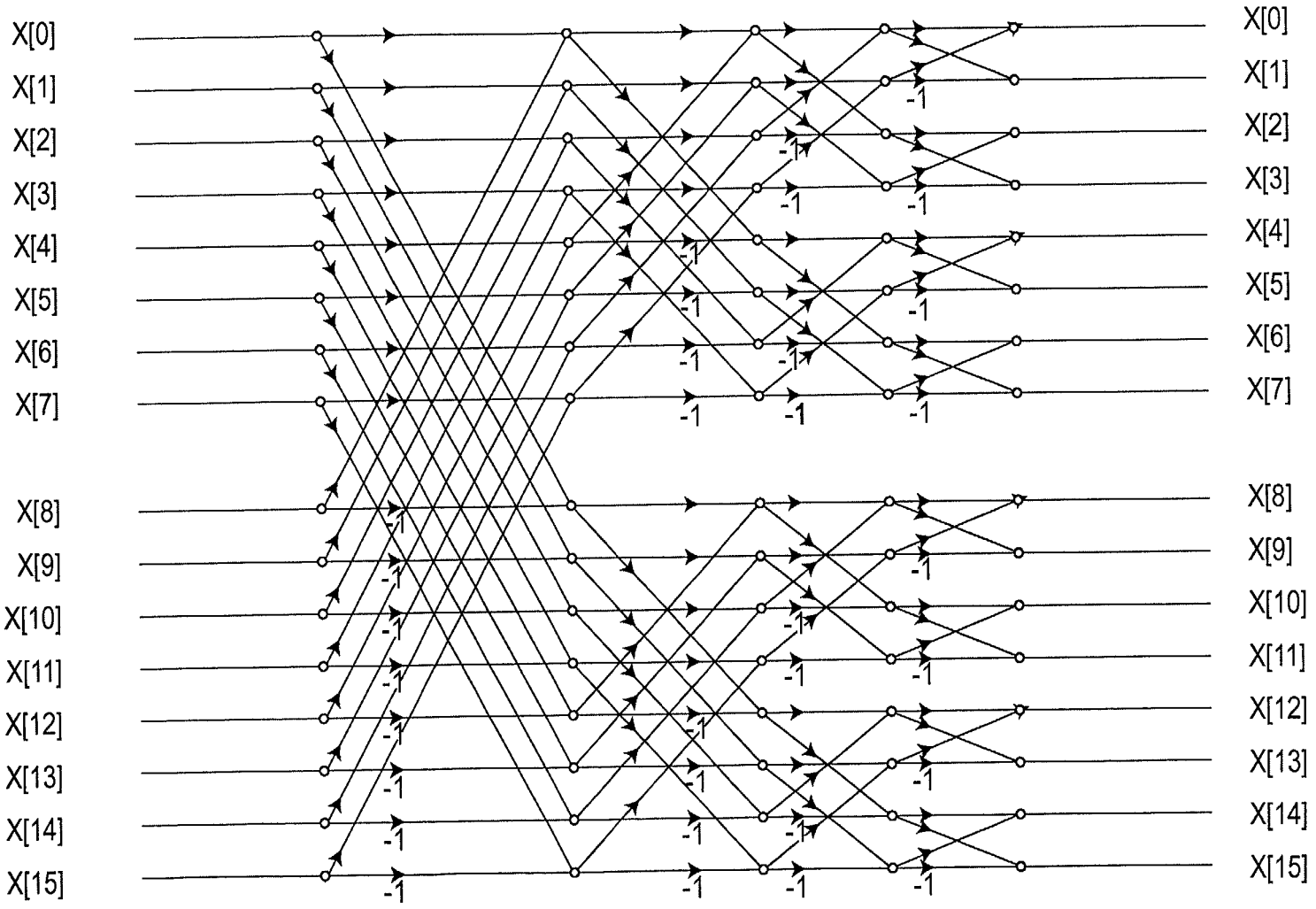


FIG. 5



FAST HADAMARD TRANSFORM STRUCTURE

FIG. 6

ELEMENTS OF FHT OUTPUT

$$\text{INPUT MATRIX} = \begin{bmatrix} x_{1,1} & x_{1,2} & \cdot & \cdot & \cdot & x_{1,16} \\ x_{2,1} & x_{2,2} & \cdot & \cdot & \cdot & x_{2,16} \\ \cdot & \cdot & x_{i,j} & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ x_{15,1} & x_{15,2} & \cdot & \cdot & \cdot & x_{15,16} \end{bmatrix}_{15 \times 16}$$

i = 1,2,3,.....15 SLOTS
j = 1,2,3,.....16 ELEMENTS PER SLOT FROM HGC OUTPUT

FIG. 7

$$\text{CODE GROUP MATRIX (KNOWN MATRIX)} = \begin{bmatrix} 1 & 1 & 2 & 8 & \cdot & \cdot & \cdot & 15 & 7 & 16 \\ 1 & 1 & 5 & 16 & \cdot & \cdot & \cdot & 14 & 12 & 10 \\ \cdot & \cdot & \cdot & \cdot & x_{i,j} & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ 9 & 12 & 10 & 15 & \cdot & \cdot & \cdot & 12 & 16 & 10 \end{bmatrix}_{64 \times 15}$$

i = 1,2,3,.....64 GROUPS
j = 1,2,3,.....15 SLOTS
$x_{i,j}$ = S-SCH CODES. ONE OUT OF 16 PER SLOT.

FIG. 8

$$\text{CORRELATION MATRIX} = \begin{bmatrix} c_{0,0} & c_{0,1} & \cdot & \cdot & c_{0,14} \\ c_{1,0} & c_{1,1} & \cdot & \cdot & c_{1,14} \\ \cdot & \cdot & c_{i,j} & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ c_{63,0} & c_{63,1} & \cdot & \cdot & c_{63,14} \end{bmatrix}_{64 \times 15} \text{ PER FRAME}$$

$c_{i,j} = \underset{k}{\text{INPUT MATRIX [k][CODE GROUP MATRIX[i][k]]}}$

i = 0,1,2,.....63 GROUPS
j = 0,1,2,.....14 CYCLIC SHIFTS RESPECT TO COLUMNS (SLOT OFFSETS).
k = 0,1,2,.....14 SLOTS PER FRAME.

FIG. 9

EP 2 320 576 A2 20110511

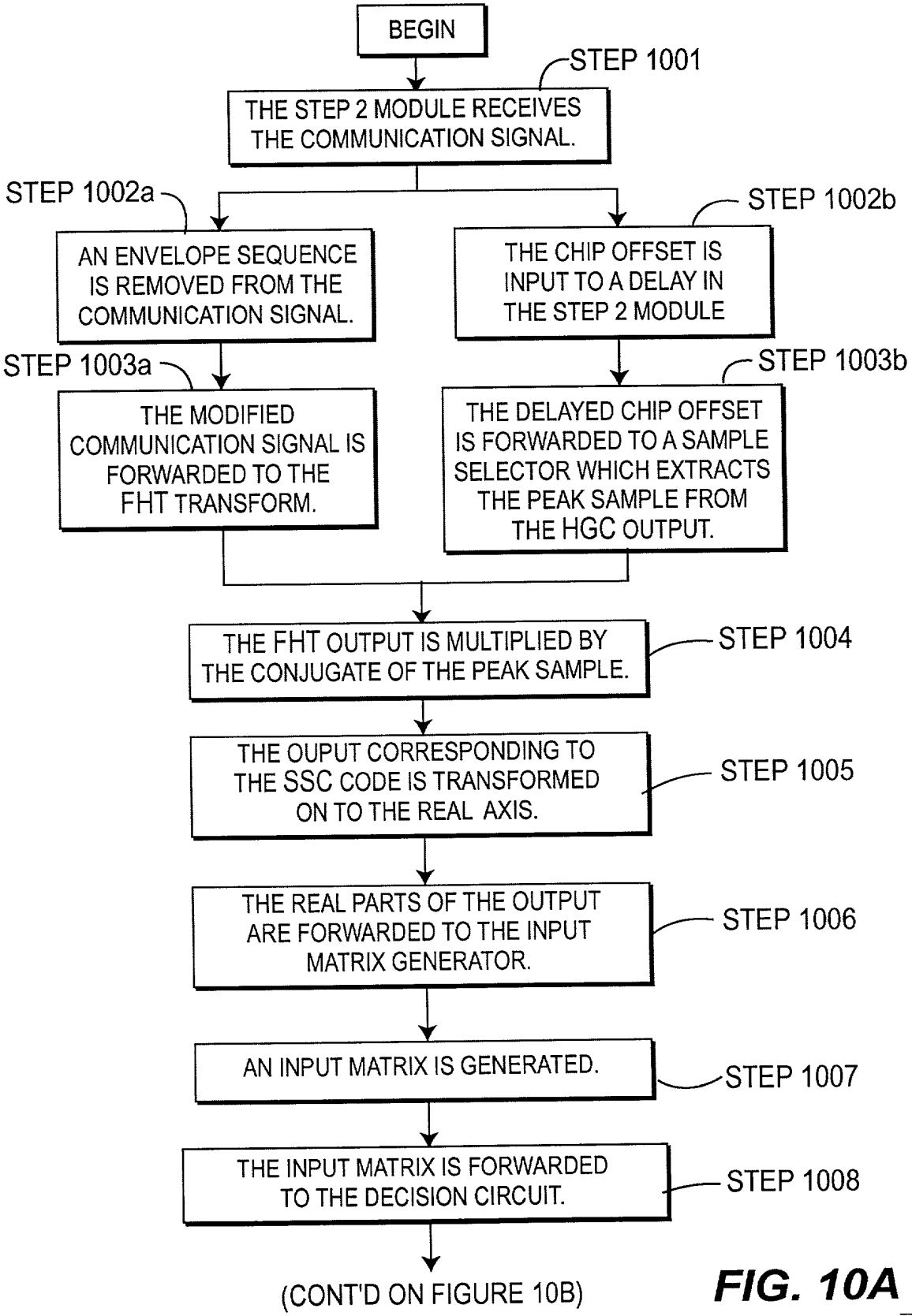


FIG. 10A

EXPRESS MAIL NO. EV325976004

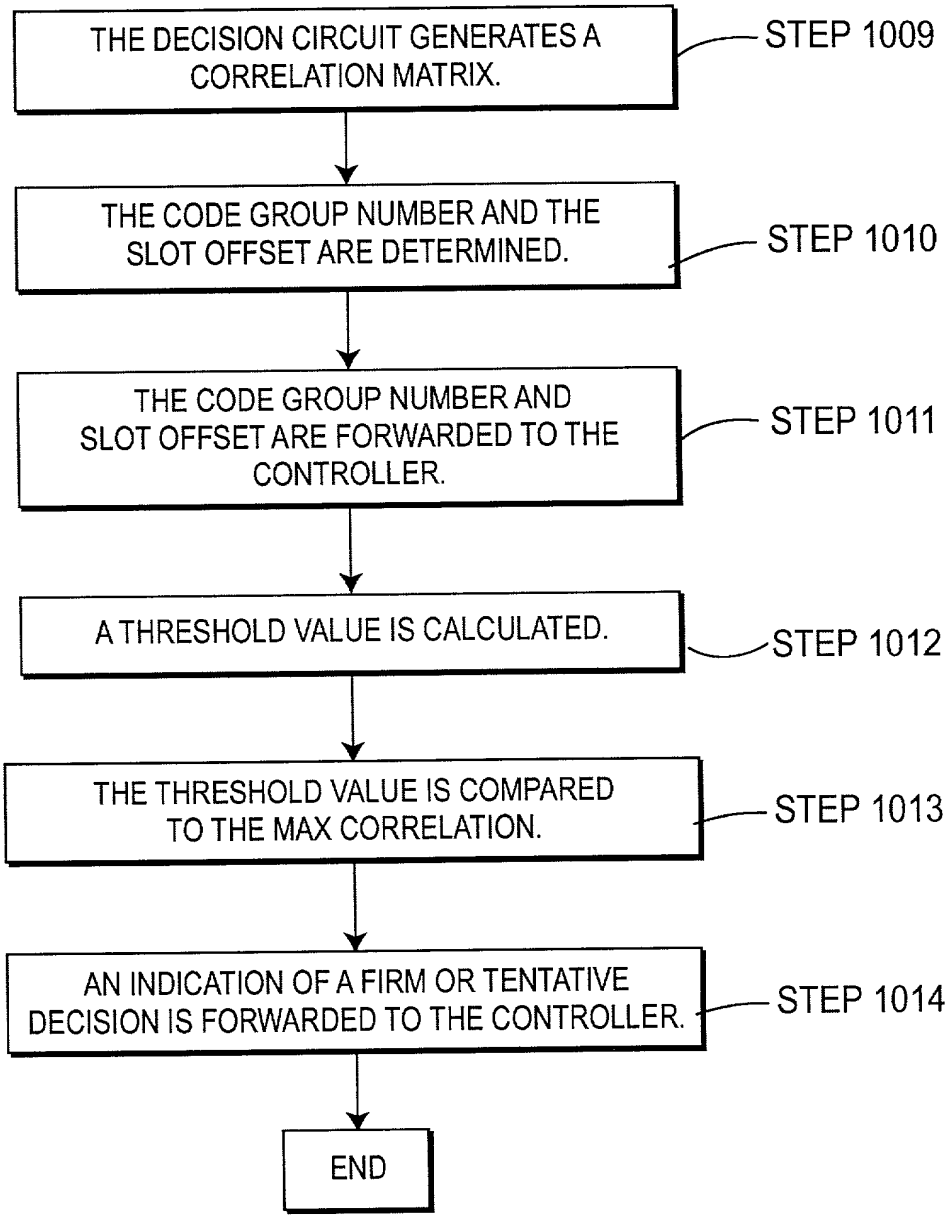


FIG. 10B

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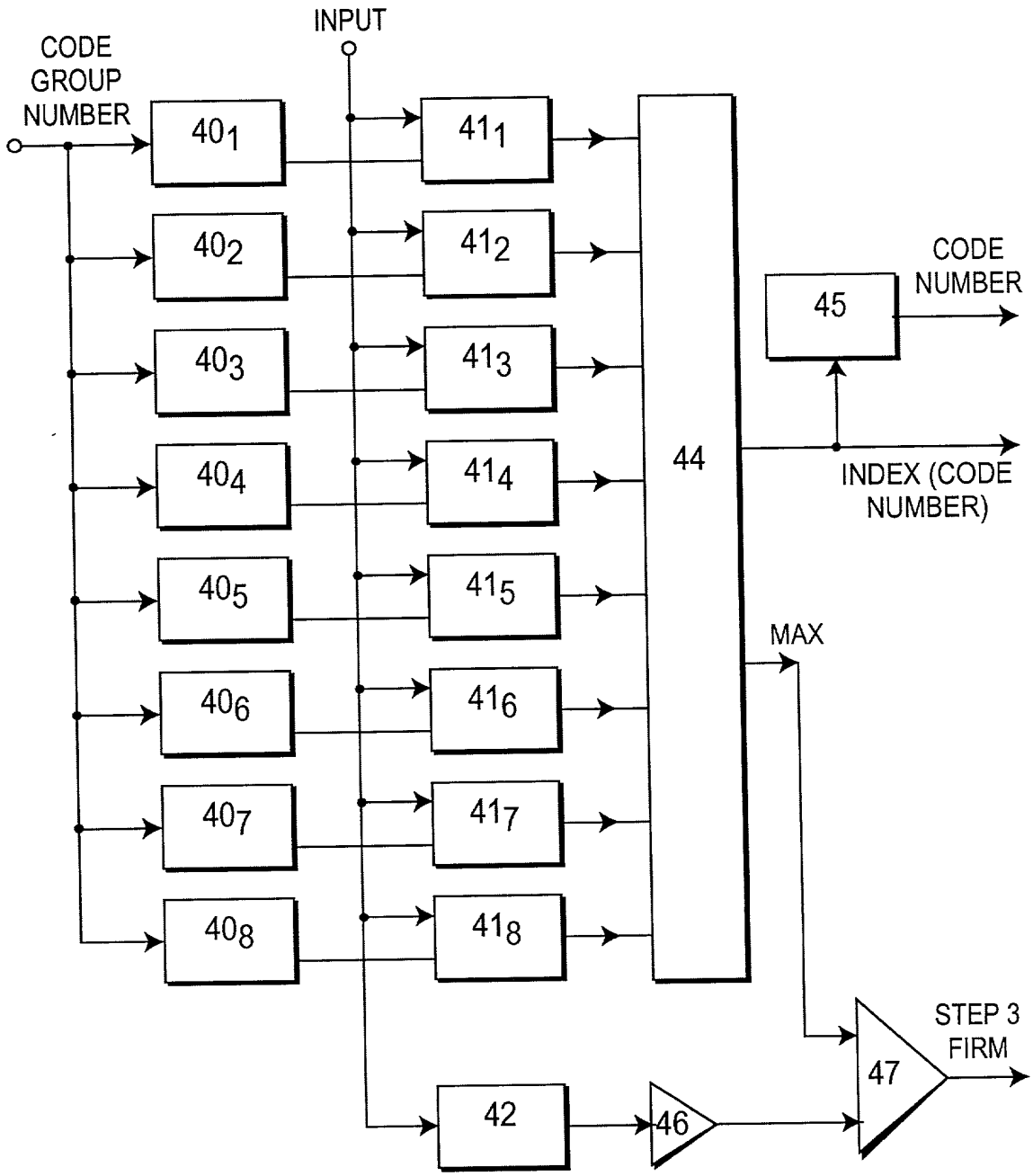
INPUT
CODE GROUP NUMBER
401
402
403
404
405
406
407
408
411
412
413
414
415
416
417
418
44
45
CODE NUMBER
INDEX (CODE NUMBER)
MAX
42
46
47
STEP 3 FIRM

FIG. 11

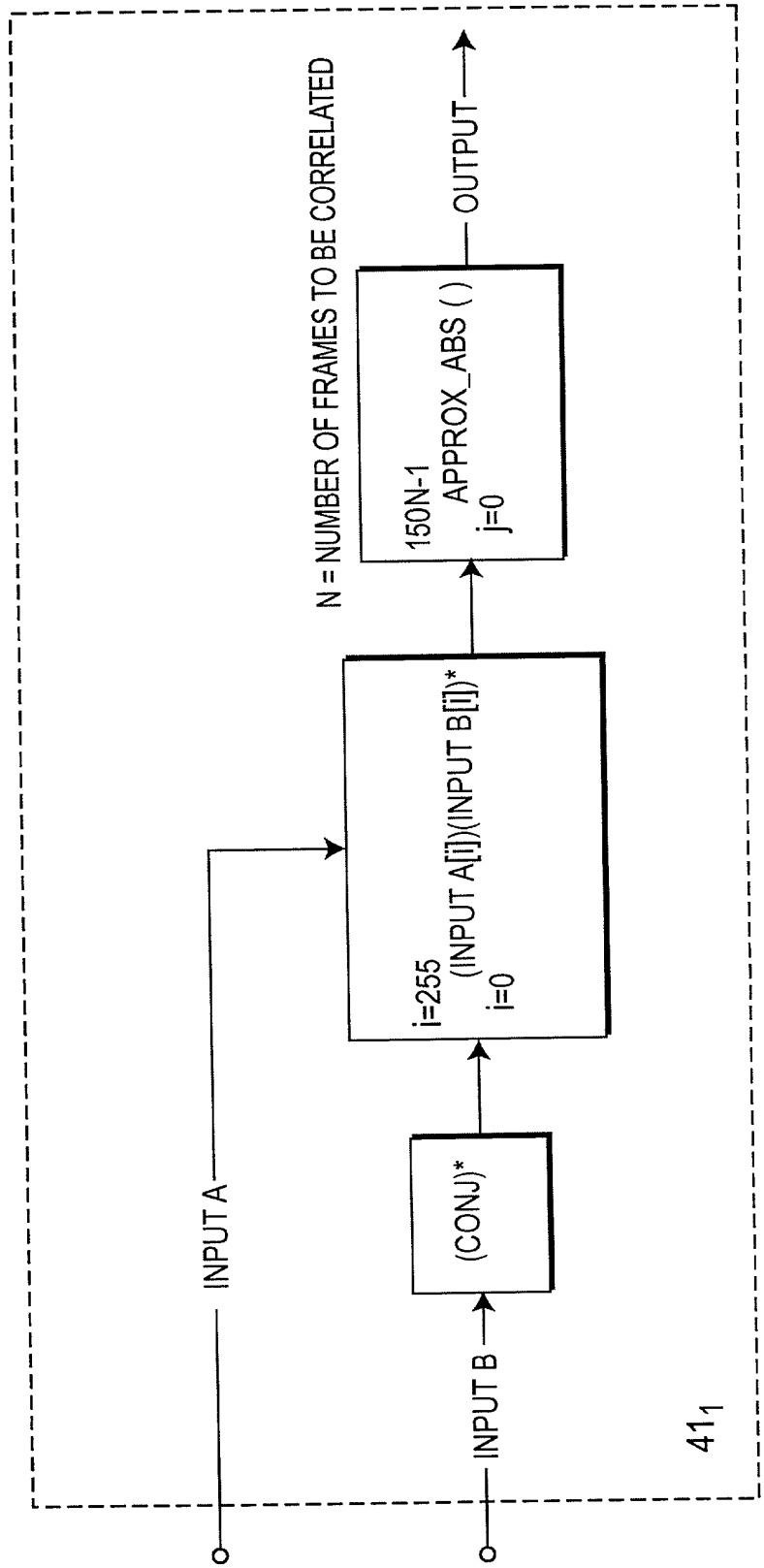
INPUT A
INPUT B
(CONJ)*
i=255
(INPUT A[i])(INPUT B[i])*
i=0
150N-1
APPROX_ABS ( )
j=0
N = NUMBER OF FRAMES TO BE CORRELATED
OUTPUT
41 1

FIG. 12

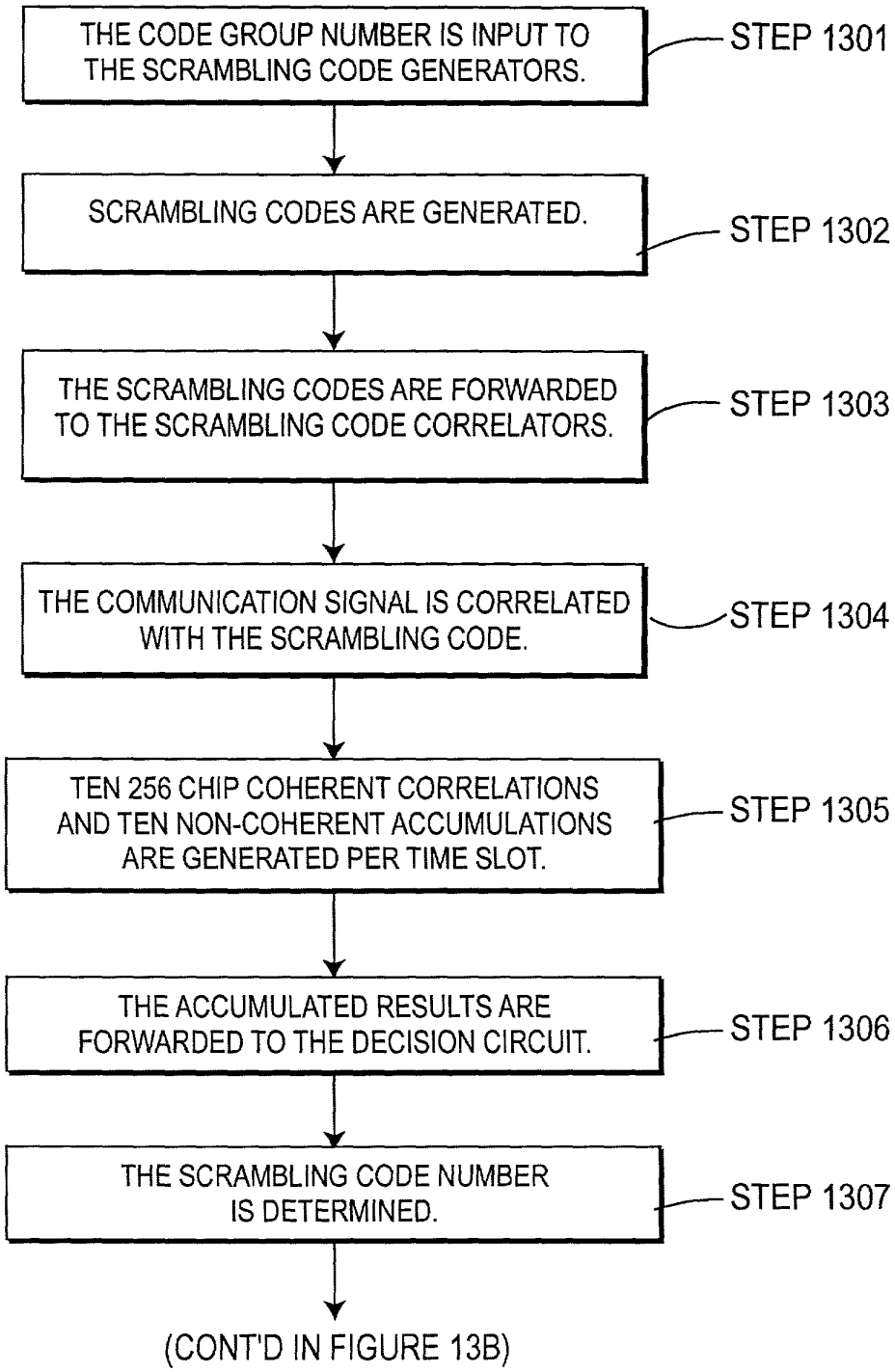

FIG. 13A

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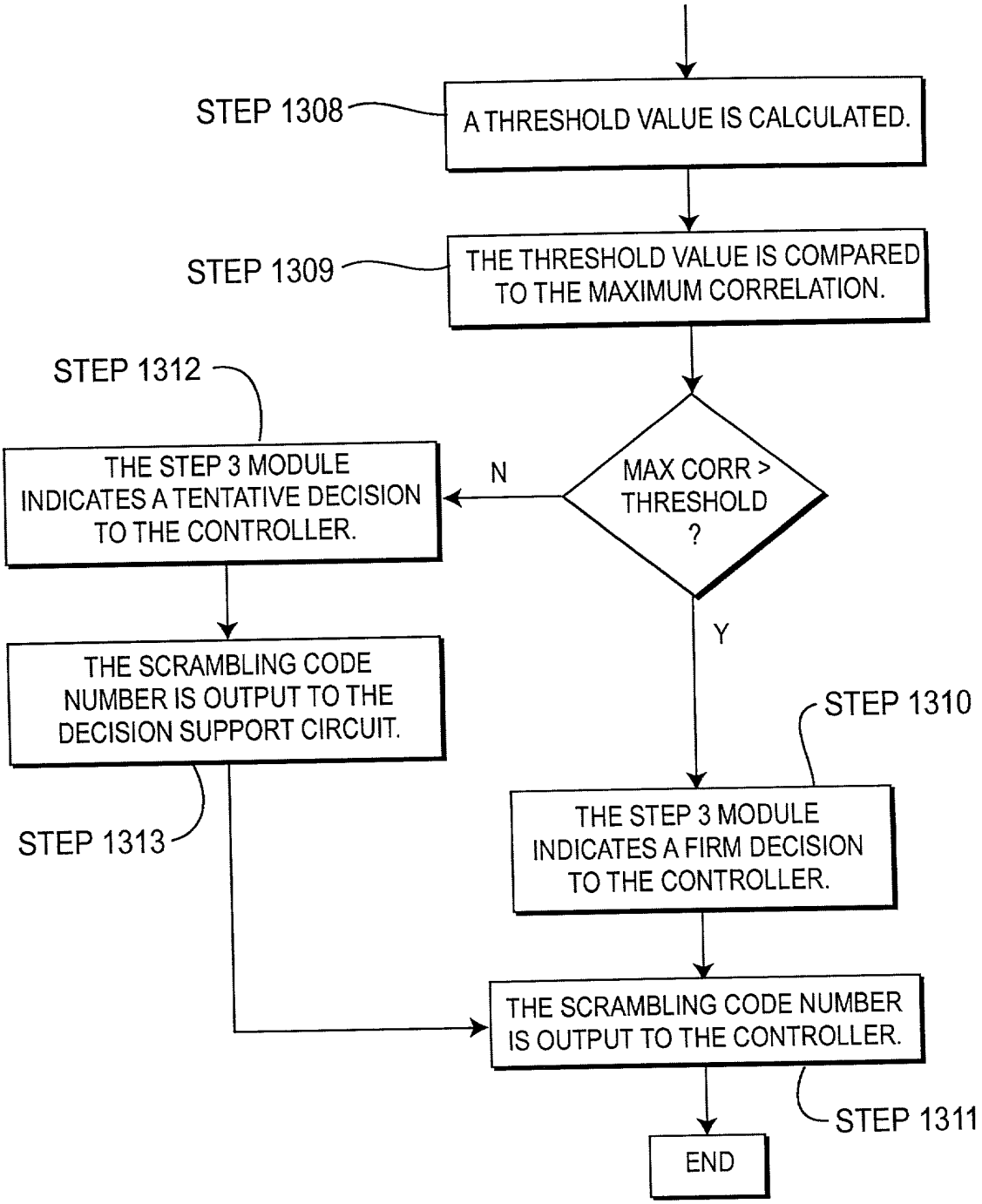

STEP 1308
A THRESHOLD VALUE IS CALCULATED.
STEP 1309
THE THRESHOLD VALUE IS COMPARED TO THE MAXIMUM CORRELATION.
MAX CORR > THRESHOLD ?
N
Y
STEP 1312
THE STEP 3 MODULE INDICATES A TENTATIVE DECISION TO THE CONTROLLER.
THE SCRAMBLING CODE NUMBER IS OUTPUT TO THE DECISION SUPPORT CIRCUIT.
STEP 1313
STEP 1310
THE STEP 3 MODULE INDICATES A FIRM DECISION TO THE CONTROLLER.
THE SCRAMBLING CODE NUMBER IS OUTPUT TO THE CONTROLLER.
STEP 1311
END

FIG. 13B

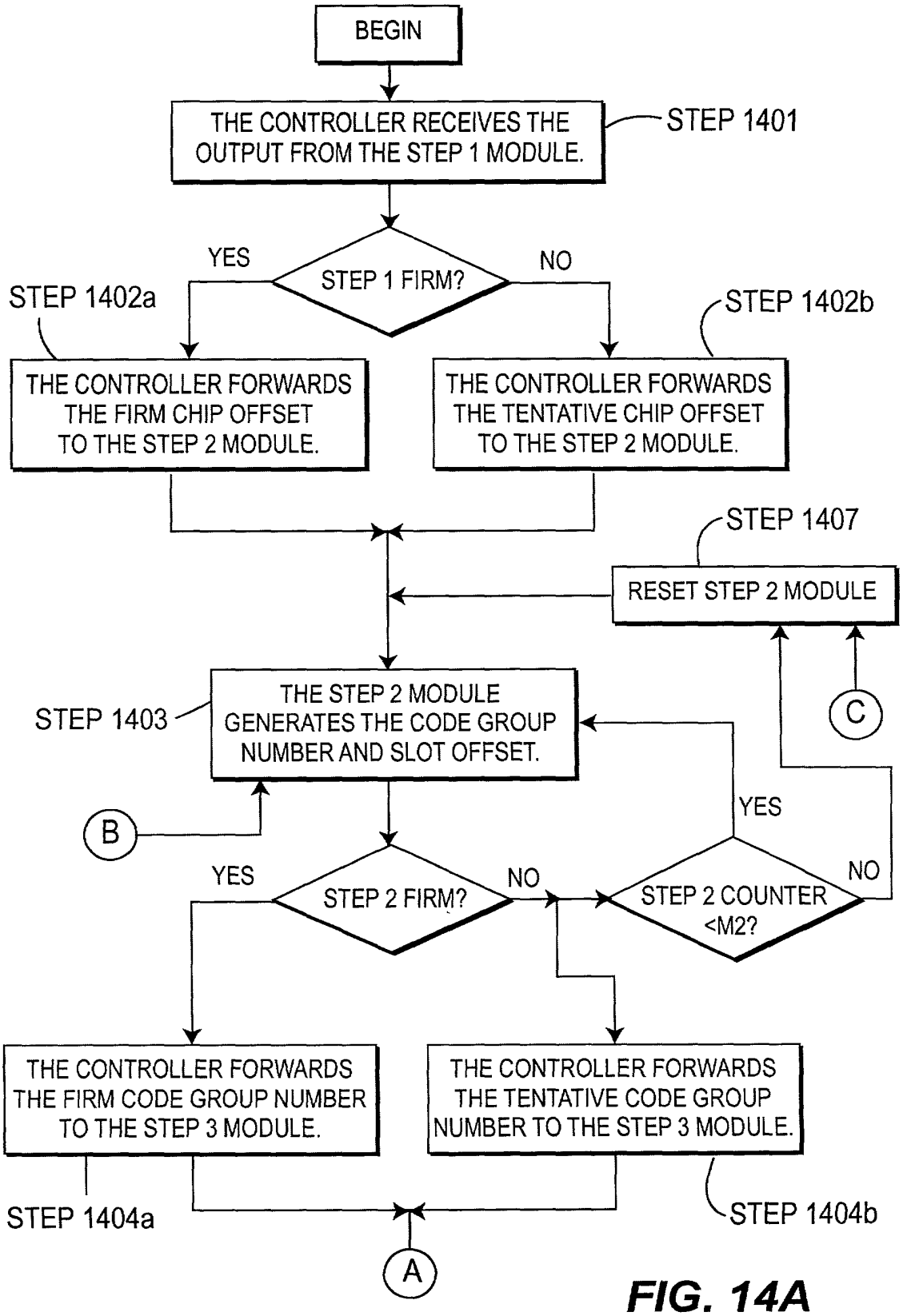


FIG. 14A

20070226-5695-0008

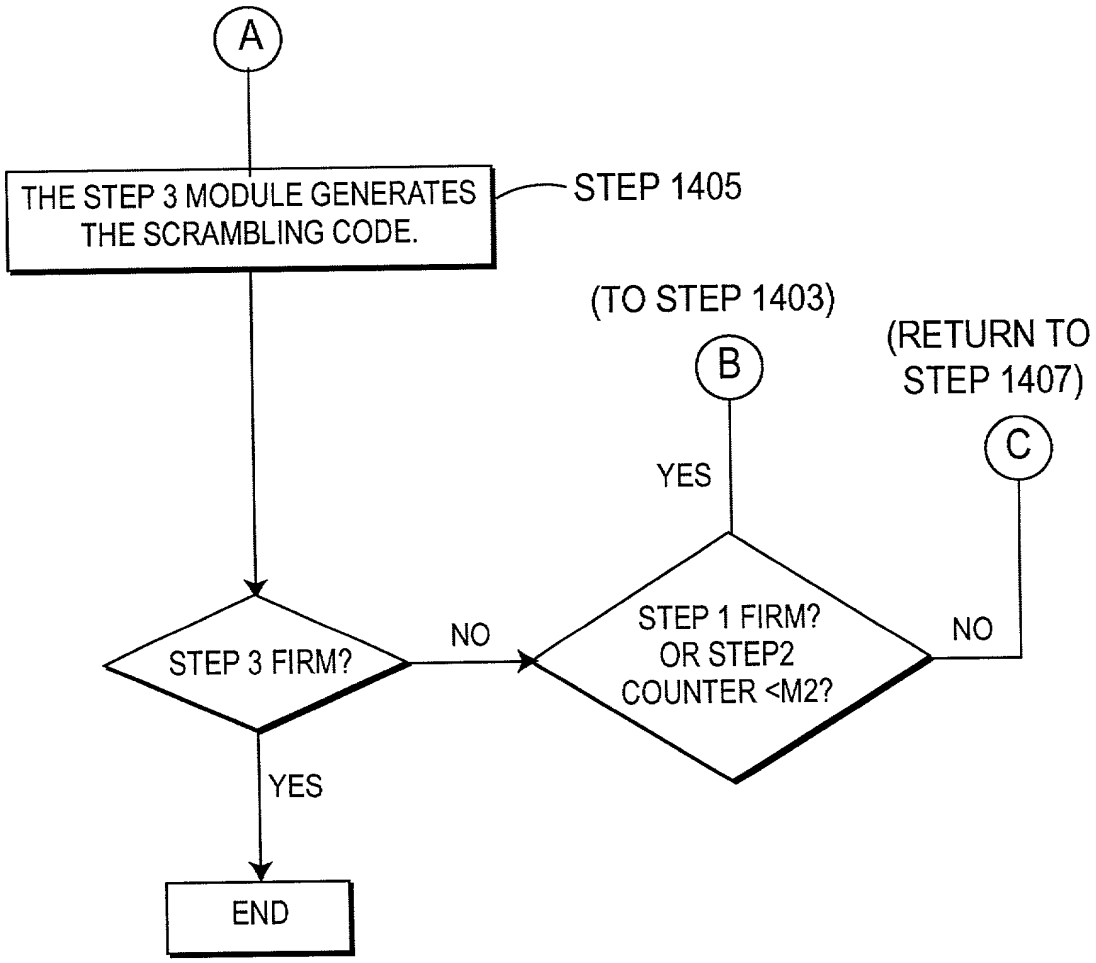

A
THE STEP 3 MODULE GENERATES THE SCRAMBLING CODE.
STEP 1405
(TO STEP 1403)
B
(RETURN TO STEP 1407)
C
YES
STEP 3 FIRM?
NO
STEP 1 FIRM? OR STEP2 COUNTER <M2?
NO
YES
END

FIG. 14B

20220"9678800T

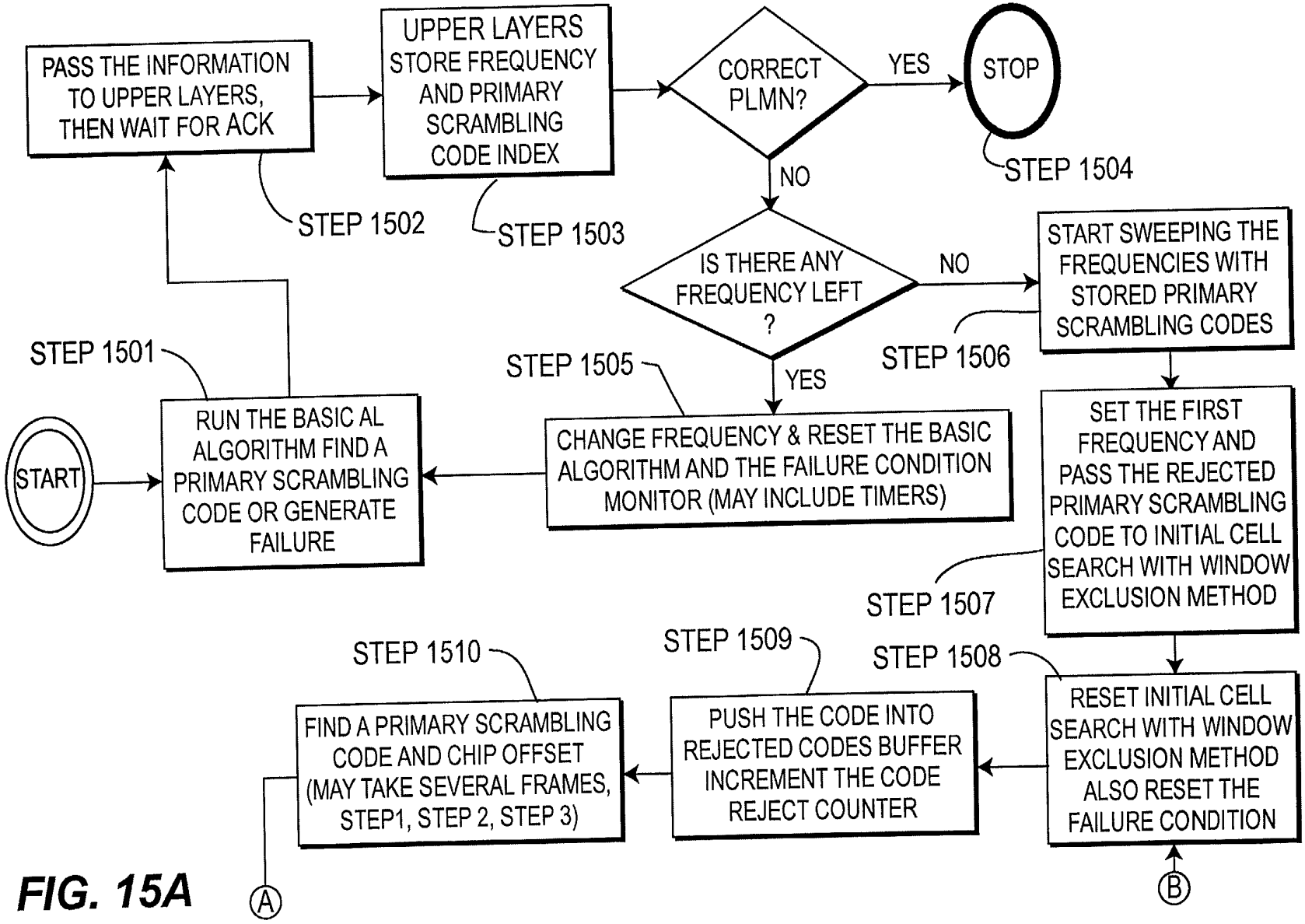
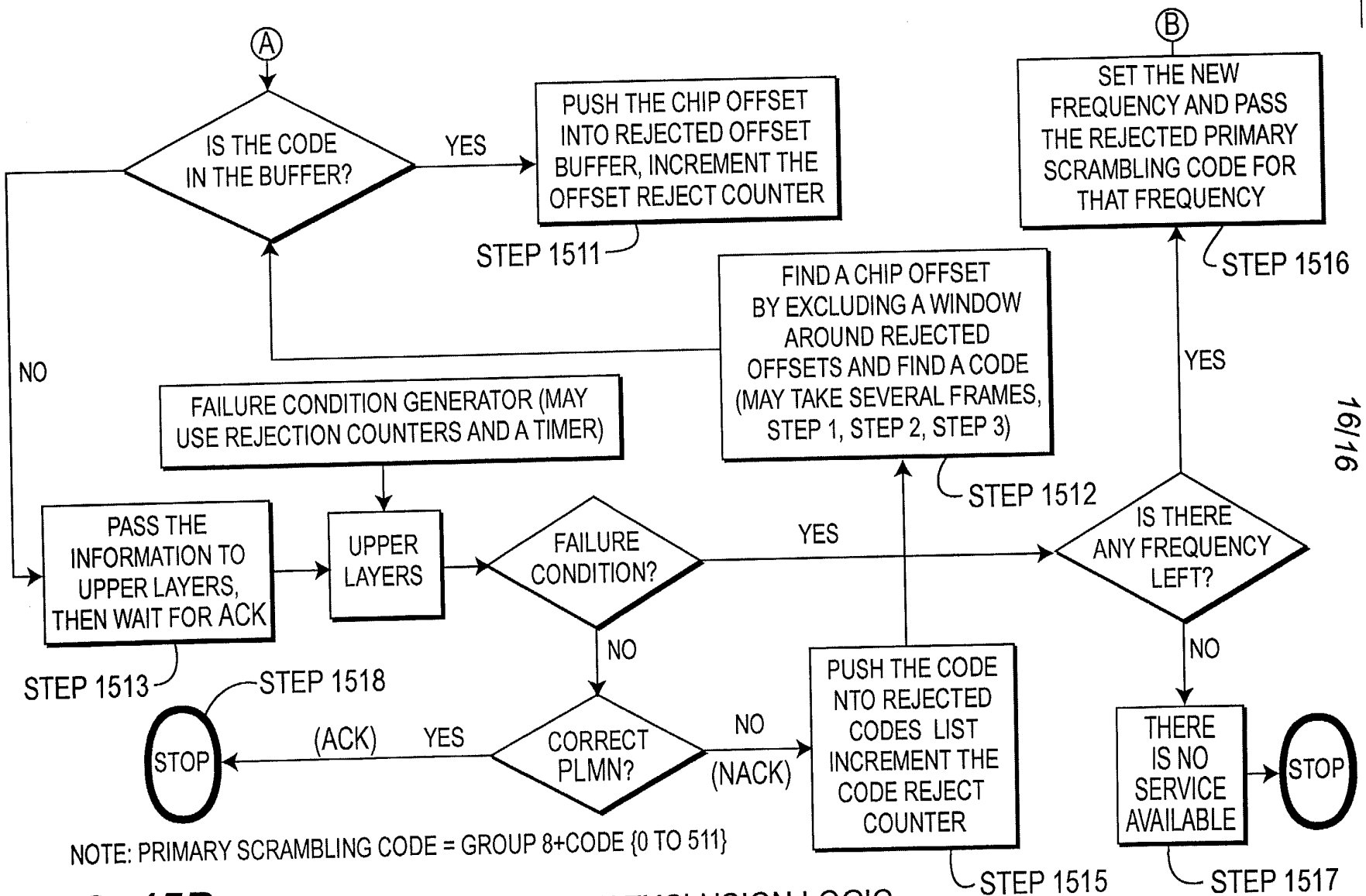


FIG. 15A



NOTE: PRIMARY SCRAMBLING CODE = GROUP 8+CODE {0 TO 511}

FIG. 15B WINDOW EXCLUSION LOGIC